forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

25. (Amended) A method of fabricating a memory array, the method comprising the steps of:

epitaxially forming a first conductivity type first source/drain region layer on an unbonded substrate;

epitaxially forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

forming a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array;

[without forming an ion implanted barrier layer in the substrate], filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the access transistors on each column.

41. (Amended) A method of forming an array of memory cells, the method comprising:

forming using a single unbonded substrate a plurality of isolated vertical access transistors separated by trenches [having no ion implanted diffusion barriers formed therein], <u>the transistors</u> comprising in order outward from the substrate, a first source drain region, a body

region and a second source/drain region, wherein the separation of trenches is such that the area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

forming a trench capacitor for each memory cell, wherein a portion of the first source/drain region serves as a first plate of the capacitor;

forming two word lines in select trenches, with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming bit lines that interconnect select second source/drain regions.

49. (Amended) A method of forming an array of memory cells, the method comprising:

forming with a single unbonded substrate a first layer of a first conductivity type of single crystalline silicon, a second layer of a second conductivity type of single crystalline silicon, and a third layer of the first type of single crystalline silicon atop the second layer;

selectively etching through the third through first layers and partially into the substrate so as to form a plurality of trenches and pillars spaced apart such that the surface area occupied by each memory cell is $4F^2$, wherein F is a minimum feature size;

[without forming an ion implanted barrier layer in the substrate,] filling the trenches with a conductive material so as to provide for a common plate for capacitors associated with each memory cell, such that a portion of the first layer in each pillar serves as a plate for the capacitor;

electrically interconnecting select pillars by word lines electrically coupled to the second layer of the select pillars; and

electrically interconnecting the select pillars by bit lines electrically coupled to the third layer of the select pillars.

51. (Amended) A method of fabricating an array of memory cells, the method comprising:

forming, using a single unbonded substrate, spaced apart access transistors isolated by trenches, each access transistor comprising in order from the substrate outward, an N+ - doped first source/drain region, a P- doped body region and an N+ -doped second source/drain region;

forming capacitors in the trench corresponding to each access transistor, wherein a portion of the N+ -doped first source/drain region adjacent the substrate serves as a plate for the

capacitor corresponding to each access transistor [, without forming an implanted barrier layer in the substrate]; and

electrically connecting the access transistors in a manner that allows for an electrical charge to be accessed or stored in each capacitor via the corresponding transistor.

53. (Amended) A method of forming a memory device having an array of memory cells and a minimum feature size F, comprising:

forming using a single unbonded substrate a plurality of vertical access transistors separated by trenches and laid out in a substantially checker-board pattern such that the memory cells occupy an area of $4F^2$, wherein the formation of the vertical access transistors consists of the steps forming a first source/drain region of a first dopant type, forming a body region of a second dopant type atop the first source/drain region, and forming a second source/drain region of a second dopant type atop the body region;

forming a capacitor in the trenches by lining the trench with a gate oxide [without forming an implanted barrier layer in the substrate], and then filling the trench with polysilicon of the first type so as to surround a portion of the first source/drain region such that the surrounded portion of the first source/drain region serves as a first plate of the capacitor and the polysilicon in the trench serves as a second plate of the capacitor; and

electrically connecting the transistors via bit lines and word lines so as to provide the capability of accessing a charge stored in one or more of the capacitors or providing a charge thereto.

55. (Amended) A method of forming an electronic device having an array of memory cells and a minimum feature size F, comprising:

forming with a single unbonded substrate a plurality of spaced apart access transistors each comprising in order outward from the substrate, a first layer of N+ dopant serving as first source/drain, a second layer of P- dopant serving as a body region and a third layer of N+ dopant serving as a second source/drain region;

wherein the forming of the access transistors includes the step of forming trenches

therebetween so as to provide a memory cell area of $4F^2$;

forming, for each transistor, a capacitor in the trenches by filling the trench with a thin layer of oxide and polysilicon [without forming an ion implanted barrier layer in the substrate], such that a portion of the first source/drain, the oxide layer and the polysilicon respectively serve as a first plate, a dielectric, and a second plate for the capacitor

electrically connecting the transistors with word lines and bit lines;

connecting the word lines to a word line decoder;

connecting the bit lines to a bit line decoder;

operatively connecting the word line and bit line decoders to an address buffer; and

interfacing the address buffer to an electronic system via address lines.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 22, 2002, and the references cited therewith.

Claims 20, 25, 41, 49, 51, 53 and 55 are amended; as a result, claims 20-56 remain pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on February 21, 2002, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§112 Rejection of the Claims

Claims 20-56 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.